US 5,786,700 similarly determines the linear interconnection resistance between two external access points of an electronic device. Various currents or voltages are injected between the two access points, so as to forward bias an internal ESD diode, and resultant voltages or currents measured. The resultant current-voltage relationships are applied to an interconnection model algorithm to yield an interconnection resistance.

Whilst the above two methods may be useful in determining values for dynamic and static series resistance, neither of these two quantities has any intrinsic importance in the detection of unconnected device pins, especially in cases having more than one device connection on a net.

Rather, it is desirable to detect pin connection failures reliably, in the presence of unknown series resistance in the test path.

According to a first aspect of the present invention there is provided a method of testing the integrity of a plurality of semiconductor device connections where each semiconductor device includes a non-linear element in a conduction path between a first node where a test signal is injected and a second node connected to a power supply connection of the devices; the method comprising the steps of: applying a test signal to the devices such that a test current flows between said nodes creating a voltage difference between said nodes, making measurements of the voltage difference as the test current varies, and on the basis of the measurements extracting a response component due predominantly to the non-linear characteristic of the devices and using this to indicate whether the connections to the devices are acceptable.

It is thus possible to provide a method which can test the integrity of device connections to a substrate, such as a circuit board, even when a plurality of devices are connected in parallel to the same test connection, and which is substantially independent of series resistance in the test path.

Preferably the test signal is a DC current generated by a current source, the changes in voltage resulting in changes in the current may then analysed so as to calculate a dynamic

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differences occurring between the first group of pins and a reference voltage; applying one or more second test signals to the second group of pins and measuring one or more respective second voltage differences occurring between the second group of pins and a reference voltage; and on the basis of measurements extracting and comparing a non-linear characteristic of the first and second group of pins to obtain a measure of continuity.

Advantageously the groups are selected such that each should perform in the same way under test, i.e. similar numbers of similar device connections are in each group.

According to a third aspect of the present invention there is provided an apparatus for testing the integrity of a plurality of device connections where each device includes a non-linear element in a conduction path between a first node where a test signal is injected and a second node connected to a power supply connection of each device, the apparatus comprising: signal means for applying a test signal to the devices such that a test current flows between said nodes creating a voltage difference between said nodes, a voltage measuring device for making measurements of the voltage difference as the test current varies, and a data processor arranged on the basis of the measurements to extract a response component due predominantly to the non-linear characteristic of the devices and using this to indicate whether the connections to the devices are acceptable.

According to a fourth aspect of the present invention there is provided an apparatus for testing the continuity of connections in a circuit path comprising a plurality of integrated circuit device pins forming a first group connected to a first circuit node such that current flows via the pins and through associated semiconductor junctions to a second circuit node, the apparatus comprising: first signal means for applying M test signals to the first group of pins and measuring M voltage differences occurring between the first circuit node and a reference, where M is an integer greater than zero; second signal means for applying N test signals to a second group of pins expected to have a behaviour identical to or relatable to the first group of pins and measuring N voltage differences occurring between a second circuit node connected to the second group of pins and a reference, where N is an integer greater than zero; and a processor responsive to the voltage differences for deriving or

comparing a non-linear characteristic of the first and second groups of pins to obtain a measure of continuity.

Preferably the non-linear characteristic is a dynamic offset voltage or a real or synthetic harmonic content.

Preferably M and N are equal and identical test signals are applied concurrently to the first and second groups of pins.

Preferably the difference in non-linear characteristic between the first and second group of pins used as a measure of continuity is calculated directly from respective differences in measured M and N voltage differences.

The M and N signals may be samples from a regularly sampled sinusoidal or other waveform having little or zero low-order harmonic content

The present invention will further be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a graph illustrating the current-voltage characteristic of a diode;

Figure 2 illustrates the voltage contributions of a linear and non-linear device in series;

Figure 3 illustrates the voltage contributions of a resistor and diode in series;

Figure 4 illustrates the effective equivalence of a plurality of diodes in parallel, with a single larger diode;

Figure 5 schematically illustrates the circuit of a tester constituting an embodiment of the present invention;

Figure 6 shows an equivalent circuit of the arrangement shown in Figure 5;

CLAIMS

1. A method of testing the integrity of a plurality of semiconductor device connections where each semiconductor device includes a non-linear element in a conduction path between a first node where a test signal is injected and a second node connected to a power supply connection of the devices; the method comprising the steps of:

applying a test signal to the devices such that a test current flows between said nodes creating a voltage difference between said nodes,

making measurements of the voltage difference as the test current varies, and

on the basis of the measurements extracting a response component due predominantly to the non-linear characteristic of the devices and using this to indicate whether the connections to the devices are acceptable.

2. A method as claimed in claim 1, in which measured voltage difference values and their respective test current values are analysed to calculate an offset voltage for the dynamic resistance of the circuit.

3. A method as claimed in claim 2, wherein the non-linear devices are diodes and the offset voltage is a function of the number of diodes passing the current between the first and second nodes.

4. A method as claimed in any preceding claim in which the test signal is supplied from a current source.

5. A method as claimed in claim 1, in which the test signal comprises a DC signal of switchable value.

6. A method as claimed in claim 1, in which the test signal comprises an AC signal.

7. A method as claimed in claim 6, in which harmonics of the AC signal generated by virtue of current flow in the non-linear devices are detected in order to indicate the presence of the non-linear devices.

8. A method as claimed in claim 7, in which the magnitude of a harmonic component is used as a measure of the number of non-linear devices connected between the first and second nodes.

9. A method as claimed in claim 1 in which the test signal comprises discrete time samples of a sinusoidal or other waveform having little or zero low-order harmonic content, and the measured voltage differences are used as discrete samples in reconstructing the response to a sinusoidal or other waveform having little or zero low-order harmonic content input for harmonic analysis.

10. A method of testing the continuity of a connection between an integrated circuit pin and a circuit board where the integrated circuit pin is connected to a plurality of integrated circuit pins forming a first group, the method comprising the steps of:

identifying a second group of integrated circuit pins having electrical properties relatable to the first group;

applying one or more first test signals to the first group of pins and measuring one or more respective first voltage differences occurring between the first group of pins and a reference voltage;

applying one or more second test signals to the second group of pins and measuring one or more respective second voltage differences occurring between the second group of pins and a reference voltage; and

on the basis of measurements extracting and comparing a non-linear characteristic of the first and second group of pins to obtain a measure of continuity.

11. A method as claimed in claim 10, in which the first and second groups comprise the same number of device pins.

19. An apparatus for testing the integrity of a plurality of device connections where each device includes a non-linear element in a conduction path between a first node where a test signal is injected and a second node connected to a power supply connection of each device, the apparatus comprising:

signal means for applying a test signal to the devices such that a test current flows between said nodes creating a voltage difference between said nodes,

a voltage measuring device for making measurements of the voltage difference as the test current varies, and

a data processor arranged on the basis of the measurements to extract a response component due predominantly to the non-linear characteristic of the devices and using this to indicate whether the connections to the devices are acceptable.

20. An apparatus as claimed in claim 19, in which measured voltage difference values and their respective test current values are analysed to calculate an offset voltage for the dynamic resistance of the circuit.

21. An apparatus as claimed in claim 20, wherein the non-linear devices are diodes and the offset voltage is a function of the number of diodes passing the current between the first and second nodes.

22. An apparatus as claimed in claim 19, 20 or 21, in which the test signal is supplied from a current source.

23. An apparatus as claimed in claim 19, in which the test signal comprises a DC signal of switchable value.

24. An apparatus as claimed in claim 19, in which the test signal comprises an AC signal.

25. An apparatus as claimed in claim 24, in which the harmonic components of the signal generated by virtue of current flow in at least one non-linear device are detected in order to indicate the presence of at least one non-linear device.

26. An apparatus as claimed in claim 25, in which the magnitude of a harmonic component is used as a measure of the number of non-linear devices connected between the first and second nodes.

27. An apparatus as claimed in claim 19, in which the test signal comprises discrete time samples of a sinusoidal or other waveform having little or zero low-order harmonic content, and the measured voltage differences are used as discrete samples in reconstructing the response to a sinusoidal or other waveform having little or zero low-order harmonic content input for harmonic analysis.

28. An apparatus for testing the continuity of connections to in a circuit path comprising a plurality of integrated circuit device pins forming a first group connected to a first circuit node such that current flows via the pins and through associated semiconductor junctions to a second circuit node, the apparatus comprising:

first signal means for applying M test signals to the first group of pins and measuring M voltage differences occurring between the first circuit node and a reference, where M is an integer greater than zero;

second signal means for applying N test signals to a second group of pins expected to have a behaviour identical to or relatable to the first group of pins and measuring N voltage differences occurring between a second circuit node connected to the second group of pins and a reference, where N is an integer greater than zero; and

a processor responsive to the voltage differences for deriving or comparing a non-linear characteristic of the first and second groups of pins to obtain a measure of continuity.